CURRICULUM VITAE

Personal Information				
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Research Interest

Deep learning accelerators; software-hardware codesign

Professional Memberships

PLOS ONE – Academic Editor
IEEE – Member
CCF – Member

Other Roles

Education & Working Experience

2011.08 – 2015.06 **Bachelor of Engineering** Xi'an Jiaotong University
Department of Electronic Science and Technology
2015.09 – 2021.06 **Ph.D** Hong Kong University of Science and Technology
Department of Electronic and Computer Engineering

Publications

- X. Chen*, R. Pan, X. Wang, F. Tian and C.-Y. Tsui, "Late Breaking Results: Weight Decay is ALL You Need for Neural Network Sparsification," 60th ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, USA, 2023, pp. 1-2.
- X. Chen*, J. Zhu, J.Jiang and C.-Y. Tsui, "Tight Compression: Compressing CNN Through Fine-Grained Pruning and Weight Permutation for Efficient Implementation," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 42, no. 2,

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- Xizi Chen*, Jingyang Zhu, Jingbo Jiang, Chi-Ying Tsui, “Tight Compression: Compressing CNN Model Tightly Through Unstructured Pruning and Simulated Annealing Based Permutation,” 57th Design Automation Conference (DAC), San Francisco, USA. July 20-24, 2020, 1-6.
- J. Jiang, X. Chen*, C.-Y. Tsui, “Accelerating Large Kernel Convolutions with Nested Winograd Transformation,” IFIP/IEEE 31st International Conference on Very Large Scale Integration (VLSI-SoC), Dubai, United Arab Emirates, 2023, pp. 1-6.
- X. Chen*, J. Jiang, J. Zhu, C.-Y. Tsui, “SubMac: Exploiting the Subword-Based Computation in RRAM-Based CNN Accelerator for Energy Saving and Speedup,” Integration, the VLSI Journal, 2019, 69: 356-368.
- X. Chen*, J. Zhu, J. Jiang, C.-Y. Tsui, “CompRRAE: RRAM-Based Convolutional Neural Network Accelerator with Reduced Computations Through a Runtime Activation Estimation,” 24th Asia and South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan. Jan 21-24, 2019, 133-139.
- X. Chen*, J. Jiang, J. Zhu, C.-Y. Tsui, “A High-Throughput and Energy-Efficient RRAM-Based Convolutional Neural Network Using Data Encoding and Dynamic Quantization,” 23rd Asia and South Pacific Design Automation Conference (ASP-DAC), Jeju, Korea. Jan 22-25, 2018, 123-128.
- X. Wang*, X. Liu, X. Hu, X. Zhong, X. Chen, Y. Liu, P. Kong, F. Tian and C.-Y. Tsui, “TAC-RAM: A 65nm 4Kb SRAM Computing-in-Memory Design with 57.55 TOPS/W supporting Multibit Matrix-Vector Multiplication for Binarized Neural Network,” 2022 IEEE 4th International Conference on Artificial Intelligence Circuits and Systems (AICAS), Incheon, Korea. Jun 13-15, 2022, 66-69.
- J. Zhu*, J. Jiang, X. Chen, C.-Y. Tsui, “SparseNN: An Energy-Efficient Neural Network Accelerator Exploiting Input and Output Sparsity,” Design, Automation and Test in Europe Conference and Exhibition (DATE), Dresden, Germany. March 19-23, 2018, 241-244.